

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 01162362
 PUBLICATION DATE : 26-06-89

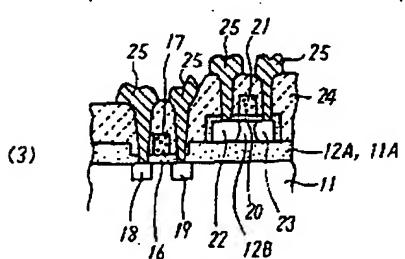
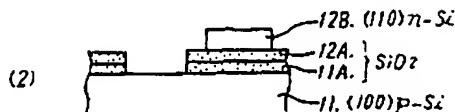
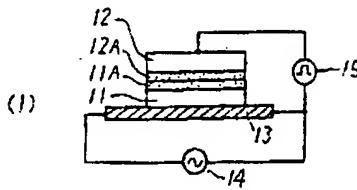
APPLICATION DATE : 18-12-87
 APPLICATION NUMBER : 62321812

APPLICANT : FUJITSU LTD;

INVENTOR : HASEGAWA MICHIEHIKO;

INT.CL. : H01L 27/08 H01L 27/00 H01L 29/78

TITLE : MANUFACTURE OF
 SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To speed up a CMOS element by a method wherein an n-channel FET with a channel region in a plane (100) is built in p-type silicon and a p-channel FET with a channel region in a plane (100) is formed in n-type silicon.

CONSTITUTION: A p-Si substrate 11 of a plane index (100) and an n-Si substrate 12 of a plane index (100), mounted with approximately 3000 μ | thick SiO₂ layers 11A and 12A, are put together on their SiO₂ surfaces and placed on a carbon heater 13. The substrates 11 and 12 are heated and then exposed to a pulse voltage for adhesion. The substrate 12 is thinned out by lapping and etching. The substrate 12 is subjected to another etching after which only an island-geometry element-forming n-Si region 12B is retained and the SiO₂ layer 12A is exposed. A p-channel FET is built on the n-Si region 12B, the SiO₂ layers 12A and 11A are locally removed for the exposure of the substrate 11 for the construction of an n-channel FET thereon. This design enhances a CMOS element in its operating speed.

COPYRIGHT: (C)1989,JPO&Japio